NEMA|dc

Low-Power display controller and multi-layer composition engine

NEMA|dc is not just an ordinary display controller, it is a real "Swiss Army Knife" which contains several smart tools and functions to compose multiple graphics and video layers by improving image quality and help to reduce the SoC power consumption.

NEMA|dc supports powerful composition features, a wide range of display interfaces and advanced proprietary frame-buffer compression technology. The core is designed to lift the workload off the Graphics Processing Unit (GPU) or the host processor (CPU), and minimize the memory bandwidth. Multiple layers can be scaled, clipped, positioned and composed on the final display by overlaying video, subtitles, graphics, cursors or application windows, with or without transparency.

Features List

- Programmable display resolutions up to 32Kx32K, including:
  - VGA, XGA, HD, Full-HD, Quad Full-HD, 4K, 8K
- Compressed framebuffer support
- Variable Frame-Rate support
- Multiple input graphics or video layers
- Powerful composition
  - Alpha blending
  - Scaling
  - Programmable size, offset and format per layer
  - Programmable stride/pitch enabling panning and clipping
- RGB to YUV(YCbCr) conversion
- Per layer palette
- Global or per layer Gamma correction
- Dithering for better results on 18-bit displays
- Fixed or programmable cursors
- Display interfaces
  - MIPI DPI,MIPI DBI-B
  - LVDS, BT.656
  - Parallel RGB and YUV
  - 3- and 4- beat serial
  - Two-Phase 12-bit
  - Programmable HSYNC, VSYNC, DE, pixel clock polarity
- Programmable event interrupt request (IRQ)

Application and Markets

NEMA|dc is designed as a flexible backend of the graphics-video path which works perfect in SoCs with GPU or in tandem with the host CPU in GPU-less systems.

The possibility to choose from three different versions of NEMA|dc makes it a perfect candidate to match the budget and suits applications spanning from ultra HD smart TVs (NEMA|dc^{700}), to high-mid-range smartphones (NEMA|dc^{400}) down to battery-limited embedded systems with simpler graphics requirements (NEMA|dc^{100}).

The Android Hardware Composer (HWC) driver allows NEMA|dc^{700} and NEMA|dc^{400} to act as a surface composer to accelerate graphics requests from the Skia-graphics library, OpenGL®, or any graphics generating application running under the Android system.

Power Savings

NEMA|dc has two smart methods to reduce significantly the system power consumption:

1)TSFBc, **Think Silicon Frame-buffer compression:** A high quality lossy and 4bpp (bits-per-pixel) fixed rate scheme, which performs in real-time and requires minimal hardware. TSFBc yields into a reduction of frame-buffer size/traffic by 400-800%, depending on the color depth. The reduction of graphics memory size due to TSFBc enables systems using only internal on-chip memory by eliminating external DDR memory.

2)SSC, Smart Surface Composer: While composing on the-fly surfaces, NEMA|dc lowers the system bandwidth by eliminating multiple memory read-write cycles and memory volume accesses, compared to a system where the GPU or CPU is entirely in charge of the composition process. SSC yields into a reduction of system bus/memory load by 40-60%, depending on the number and the format of the surfaces.

TSFBc and **SSC** combined are up to **twenty (x20) times more power efficient** than systems with a conventional display controller.

Display Controller	NEMA|dc^{100}	NEMA|dc^{400}	NEMA|dc^{700}
Resolution	Up to 1024x768	Up to 1920x1080	Up to 8k
Silicon area (mm^2@28nm)	0.02	0.02 - 0.1	0.1 - 0.5
Composition layers	1	Up to 4	Up to 7
TSFBc	✓	✓	✓

Performance

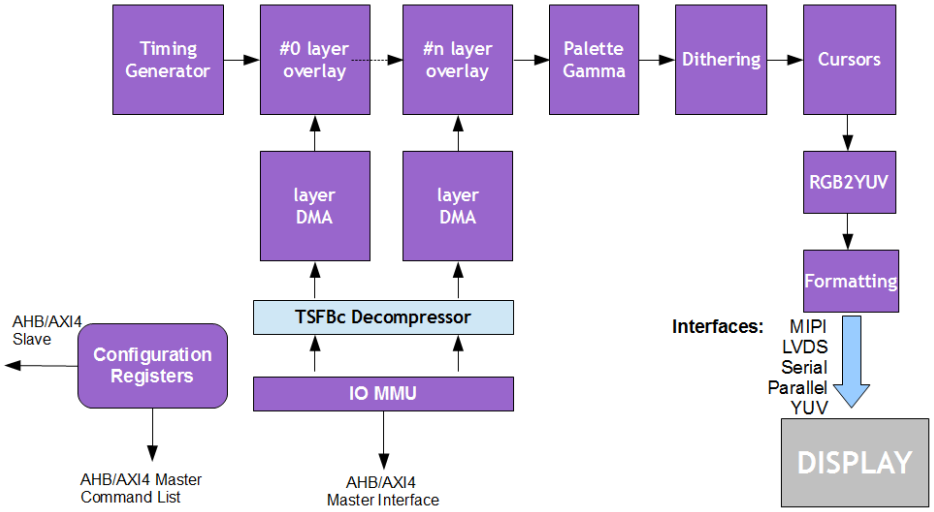
The integration of NEMA|dc allows a SoC to drive full **UltraHD** displays while operating at extremely low frequency. NEMA|dc can compose a typical case of a **four (4) layer Android user interface**, providing a smooth and seamless layer-transition experience operating only at **90MHz**. Composition and all animations are performed solely by the NEMA|dc core by moving, scaling, filtering and blending the multiple videos and graphics framebuffer layers.

Architecture

NEMA|dc is flexible and configurable while compile-time. Configuration options allowing engineers to select the number of layers, functionality of composition modules and processing methods tailored for their area requirements.

NEMA|dc can enhance the visual quality by implementing quality enhancement techniques like gamma correction and dithering.

It supports a wide range of display interfaces, such MIPI DPI/DBI, LVDS, or parallel interfaces suitable for HDMI, DisplayPort, DVI etc.



Software

- OS support
  - FreeRTOS V8.0.1
  - Linux driver 3.x
  - Android 4.x
- Graphics API support
  - Android Hardware Composer (HWC)
  - Bare-Metal Library in portable ANSI C
- Software Emulators and suites
  - NEMA|dc bit accurate emulator
  - TSFBc bit accurate emulator

Configuration Options

- DMA
  - Scanline based
  - Tile based (MIPI)
- IOMMU
- Layer Overlay
  - Number of layers
  - Scaler per layer
- Screen formatting(output encoding)
- Master Interface
  - AMBA AHB 32bit
  - AMBA AXI4 32/ 64bit
- Slave Interface
  - AMBA AHB

Software support

NEMA|dc simplifies software integration and it supports multiple OS such as RTOS, Linux, and Android. A fully documented bare metal library of primitive graphics functions is available for OS and OS-less systems. The bare metal library, written in the form of an API, is portable (pure ANSI C with no dependencies) and comes together with application-notes describing how to program NEMA|dc and enable its composition features. Driver for Android HWC (HardWare Composer) allows NEMA|dc to accelerate the hardware abstraction-level transparently to the software.

PRE-Sales Tool: The software package comes together with a bit accurate software emulator, test-suite and an additional emulator for the TSFBc compression scheme (emulators are available upon request).

Integration/verification

NEMA|dc is available in technology independent Verilog HDL and is easy to integrate and verify. NEMA|dc is silicon proven in a variety of process technologies. It is designed with AMBA interfaces (AHB, AXI 32 or 64 bit) for easy hardware integration. The core has been verified through extensive simulation and rigorous code coverage measurements. The IP comes together with a complete verification suite that compares reference images with rendered images.

Deliverables and Documentation

Deliverables includes: complete set of synthesis, STA (Static Timing Analysis) scripts, OS drivers for Linux, Android, FreeRTOS, portable bare drivers and Android HWC driver.

Documentation includes: IP manual, integration manual, software-library manual, application notes, demonstration platform, "How To Manual" with bare library application notes including programming descriptions and composition feature enablement.

A reference design systems and demo-sets are available for platforms: Xilinx Zynq, Altera SoCkit.

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