Think Silicon

ThinkLCD-ML

VGA LCD Controller

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The ThinkLCD-ML Display controller is an AMBA AHB module that can drive a VGA or LCD screen in a SoC.
Supports a configurable number of layers and image scaler per layer.
It can be easily programmed with X11 Modeline timing to support any required resolution in any step and multiple colour modes are supported.

It is a complete IP solution that includes RTL Code, elaborate testbenches, **Linux** Framebuffer Kernel **Drivers**.

ThinkLCD-ML is available for ASIC or FPGA and is specifically designed for optimal system performance with minimum power consumption and silicon area.

Multiple Layers ***Low-gate count*** ***Integrated Scaler***

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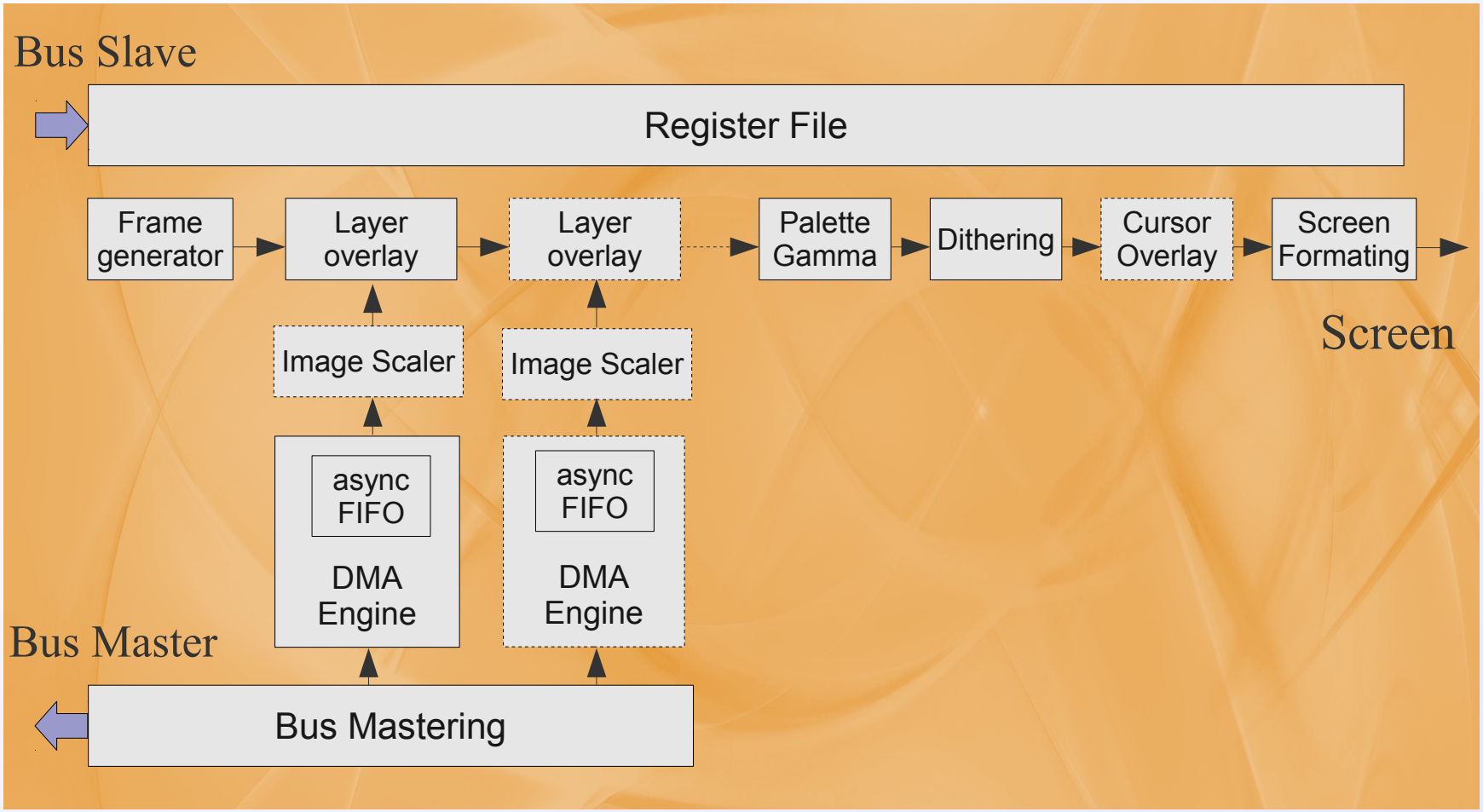
Architecture

ThinkLCD-ML



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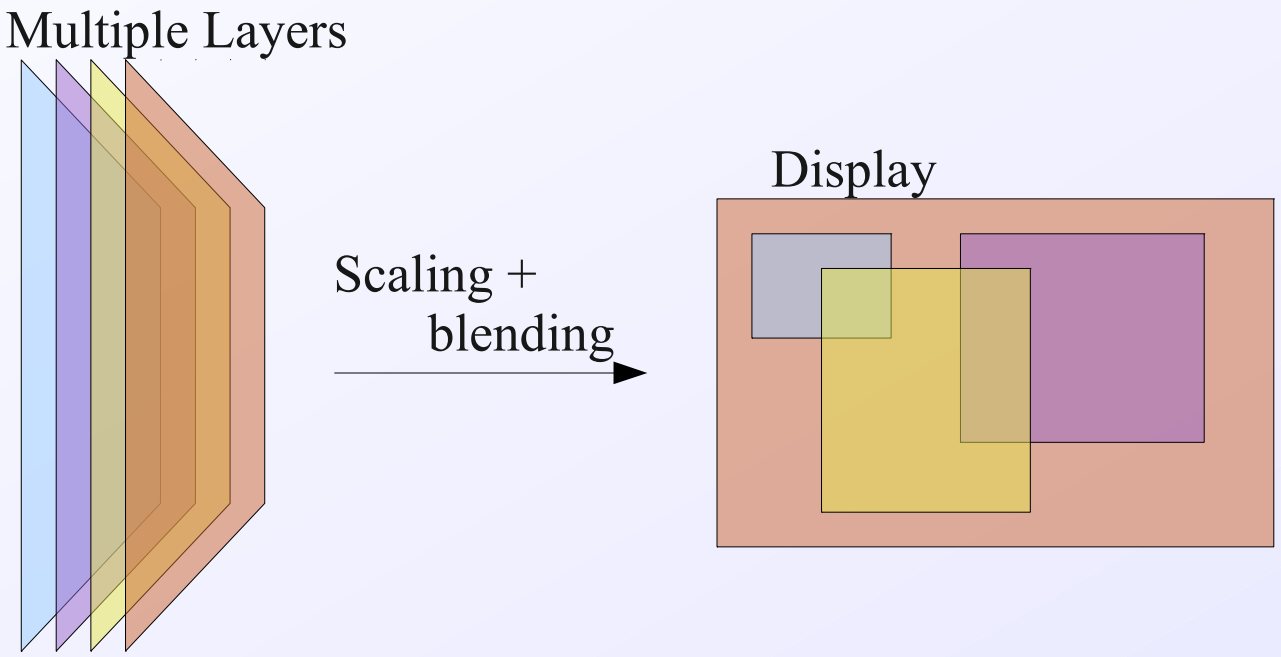
Features

Multiple Layers

- Configurable number of layers
- Blender per layer
- Optional Scaler per layer



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Features	System Requirements
Colour Format 8 bit Palette mode, 8 bit Grayscale, 8 bit mode (332) 16 bit modes (565, 555, 444) 24/32 bit modes (888) YUV **Output Format:** Parallel RGB888/666 Serial 3 RGB888/666 Serial 4 RGBX8888/6666 **Blender:** GLOBALALPHA, SRCALPHA, INVSRCALPHA, DESTALPHA, INVDESTALPHA (OpenWF) **Scaler:** Nearest Neighbour or Bilinear Filtering **Additional Features** Dithering Gamma Correction	**Interface:** 1x AHB 32-bit Master 1x AHB 32-bit Slave **Area:** ~15K gates (varies with target library and performance requirements) +10K gates per layer **Clocking:** AHB Clock Pixel Clock **Memories:** 1 dp 64x32 for DMA FIFO (configurable size) per Layer 4 tp (MaxLineSize) x 32 for DMA FIFO (configurable size) per Layer

Deliverables

VGA/LCD Controller

Hardware:
Netlist or Verilog RTL source code
Synthesis Scripts
STA Scripts

Documentation:
IP Module Description
System Integration Description
Software library Description Manual

Software:
ANSI C Source code library
Linux Framebuffer /dev/fb Drivers

Testbench:
Testing displaying test patterns and compares with expected results

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