

Mobile Graphics Solutions



Overview

ThinkVG graphics accelerator is a low area / high performance Graphics Accelerator IP Core designed to bring high performance rendering to low-gatecount embedded and mobile applications.



It is a highly balanced core that accelerates commonly used graphics functions including image transfers (blitting), image scaling, drawing primitives (filled rectangles, lines), blending, texture mapping, while its Graphics Processor is fully programmable using C/C++.

It is a complete IP solution that includes RTL Code, elaborate testbenches, Linux Framebuffer Kernel Drivers and OpenVG/Qt API Drivers.

ThinkVG is available for ASIC or FPGA and it is specifically designed for optimal system performance with low power consumption and minimum silicon area.

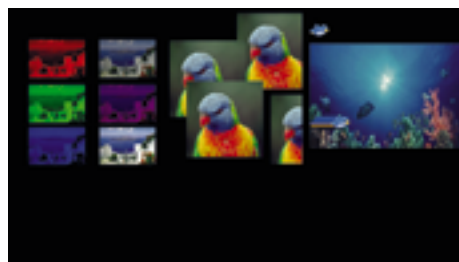
Features

- ▶ Area: 160K gates (including scan, clock gating, excluding memories)
- ▶ System Bus: available with AHB (optionally AXI)
- ▶ X4 Multisample AntiAliasing (optionally X16)
- ▶ Fill Rate : up to 2 pixels/clock cycle
- ▶ VShader: Unified SIMD floating point streaming Processor (1 core). Fully C/C++ programmable to minimise host CPU overhead
- ▶ 512-byte Instruction Cache (configurable)
- ▶ 2048-byte 64-bit Unified Data Cache/Texture Cache (configurable)
- ▶ 2K-16K Configurable GPU Scratchpad Memory
- ▶ Blender: Fully programmable streaming blending Unit
- ▶ 1 Texturing Unit supporting OpenVG formats and Compressed Textures (Point sampling / Bilinear filtering)
- ▶ Triangle Rasteriser with Gouraud Shading
- ▶ Polygon Rasterising Unit
- ▶ Direct Bezier Curve Rasterisation
- ▶ Filled Rectangles, Line, Pixel Drawing
- ▶ 2.5D Projective Image Drawing
- ▶ Blitting, Color keying, Dithering
- ▶ Image Scaling/Rotation/Mirroring, window Clipping
- ▶ 32/16/8-bit colour formats Colour conversions,
- ▶ YUY2 support for Video (optional)
- ▶ Optimised for low-gate count / low-power consumption
- ▶ OpenVG API, Linux, DirectFB drivers, Qt support

Think VG Graphics Accelerator

Core	Think VG
Resolution	any*
Speed	up to 2 pixels / clock cycle
Process	Independent RTL
Unified GPU Shader Processor	1 core
Instruction Cache	512 bytes (configurable)
Unified GPU / Texture Cache	2048 bytes (configurable)
Compiler Support	C/C++
Rectangle Fill	✓
Line Drawing	✓
Pixel Draw	✓
Triangle Draw (gouraud shaded)	✓
Bezier Polygon Rasteriser	✓
Antialiasing x 4	✓
Antialiasing x 16	optional
32 bit format RGBA8888, ARGB etc.	✓
16 bit format RGB5551, 565, 4444 etc.	✓
8 bit Grayscale, 332 etc.	✓
Blitter	✓
Composition	✓
Compressed Textures	✓
2.5D Projective Image Drawing	✓
Destination colour key	✓
Dithering support	✓
Image Scaling	✓
Porter - Duff Blending	✓
Fully Programmable Blender	✓
90, 180, 270 deg rotations	✓
Mirror X, Mirror Y	✓
Colour format conversions	✓
Negative addressing	✓
YUY2 support for video	optional
Clip Windows	✓
Configurable Endianness	O
AHB Master DMA I/f	✓
AXI Master DMA I/f	optional
Synthesizable RTL	✓
Linux Kernel Drivers	✓
DirectFB 1.4 Drivers	✓
Qt 4.8 support	✓
Open VG API Driver	✓
Available	now

✓ Standard feature, O Design Time option, - Not Available, * up to 32768 x 32768



Operating System support

- ▶ Linux
- ▶ Qt

APIs accelerated

- ▶ DirectFB 1.4
- ▶ OpenVG 1.1

Polygon Processor

- ▶ Direct rasterisation of Bezier curves
- ▶ Triangle rasterisation with gouraud interpolators

VShader

- ▶ Unified Shader Architecture minimises wasted resources and clock cycles
- ▶ Fully Programmable under C/C++
- ▶ Parallel Floating point Vector Processor
- ▶ Colour conversions
- ▶ Streaming Ports

Texture Mapping Engine

- ▶ Any texture resolution
- ▶ Any texture colour depth
- ▶ Texture Caching
- ▶ Point Sample / Bilinear texture filters
- ▶ Support for proprietary differential texture compression (4bpp) suitable for gradients

PixelBlender Processor

- ▶ Fully Programmable streaming pixel blending processor supports any blending mode
- ▶ Parallel multiplications/reciprocals
- ▶ Parallel RGB and Alpha computation units
- ▶ Gamma/Degamma support

Bus Master Interface

- ▶ AHB bus interface standard
- ▶ Optional AXI interface
- ▶ Streaming concentration ensures minimal bus bandwidth
- ▶ Configurable Endianness

General:
info@think-silicon.com

Sale inquiries
sales@think-silicon.com

www.think-silicon.com

Corporate Headquarters

Patras Science Park
Rion Achaias, 26504
Greece

Tel: + 30 2610 911543
Fax: + 30 2610 911544

Think Silicon

